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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,862	06/26/2003	Toshiki Kanamoto	239479US2	1442

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,862	KANAMOTO ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/26/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06/26/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application filed on 07/26/2003, claims 1-6 are pending.

Claim Objections

2. Claim 1 is objected to because of the following informalities: "extracted based on information related", Applicant should be more specific of what is the "information related" in the claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1- 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US 6,816,999).

5. **With respect to claim 1, Lee discloses** a parasitic capacitance extracting device for a semiconductor integrated circuit (fig. 6, step 3, col. 6, ll. 56-57), comprising:

a parasitic capacitance value information calculator configured to extract a dummy wiring pattern model from a wiring pattern library specifying wiring patterns of multilayer structure including said dummy wiring pattern model (col. 1, ll. 44-54; col. 2, ll.

38-45, and 62-65) to replace (changing) said dummy wiring pattern model with a replacing insulator (col. 3, ll. 24-33), thereby obtaining parasitic capacitance value information in which a value of a parasitic capacitance persisting said replacing insulator is in correspondence with said dummy wiring pattern model (col. 2, ll. 38-54), said replacing insulator having a dielectric constant higher than that of an interlayer insulation film isolating a wiring pattern of another layer from said dummy wiring pattern model (col. 3, ll. 28-33, 41-55, and 65-67); and

a parasitic capacitance extractor configured to receive layout pattern data specifying a semiconductor integrated circuit from which a parasitic capacitance is to be extracted (fig. 2, step 21 and 22; and col. 1, ll. 37-54) and an extraction rule for extracting a dummy wiring pattern and to extract said dummy wiring pattern from said layout pattern data (col. 6, ll. 11-31), thereby extracting a parasitic capacitance value corresponding to said dummy wiring pattern as extracted based on information related (size or timing) to said parasitic capacitance value information (col. 2, ll. 30-54; col. 7, ll. 26, ll. 16-42).

6. **With respect to claim 2, Lee discloses** the parasitic capacitance extracting device according to claim 1, further comprising regression analyzer configured to perform regression analysis on said parasitic capacitance value information to obtain regression equation information in which model size information specifying a size related to said dummy wiring pattern model is in correspondence with said parasitic capacitance value (col. 6, ll. 20-31; 38-48), wherein

said parasitic capacitance extractor includes an extractor for obtaining size information related to said dummy wiring pattern based on said layout pattern data and said extraction rule, thereby extracting a parasitic capacitance value corresponding to said size information referring to said model size information of said regression equation information(col. 2, ll. 30-54).

7. **With respect to claim 3, Lee discloses** the parasitic capacitance extracting device according to claim 1, wherein said parasitic capacitance extractor includes an extractor for obtaining said dummy wiring pattern based on said layout pattern data and said extraction rule and performing pattern matching (check) between said dummy wiring pattern and said dummy wiring pattern model in said parasitic capacitance value information, thereby extracting a parasitic capacitance value based on the result of pattern matching (col. 5, ll. 61-67; col. 6, ll. 1-18).

8. **With respect to claim 4, Lee discloses** the parasitic capacitance extracting device according to claim 1, wherein said layout pattern data is inputted to said parasitic capacitance extractor as layout pattern data in which said dummy wiring pattern is already inserted (col. 6, ll. 48-52).

9. **With respect to claim 5, Lee discloses** the parasitic capacitance extracting device according to claim 1, further comprising a dummy wiring pattern inserter configured to receive layout pattern data in which said dummy wiring pattern is not yet inserted and dummy wiring pattern insertion criteria information specifying insertion criteria of said dummy wiring pattern, thereby inserting said dummy wiring pattern in

said layout pattern in which said dummy wiring pattern is not yet inserted based on said dummy wiring pattern insertion criteria information (col5, ll. 25-40), wherein

said parasitic capacitance extractor receives said layout pattern data in which said dummy wiring pattern is inserted by said dummy wiring pattern inserter (fig. 2, col. 1, ll. 44-54).

10. **With respect to claim 6, Lee discloses** a parasitic capacitance extracting method for a semiconductor integrated circuit (abstract), comprising the steps of:

(a) receiving layout' pattern data specifying a layout structure a semiconductor integrated circuit from which a parasitic capacitance is to be extracted (fig. 2, col. 1, ll. 44-54), thereby extracting said dummy wiring pattern from said layout pattern data, said layout pattern data including a wiring pattern; pattern of multilayer structure and a dummy wiring (col. 6, ll. 11-31)

(b) replacing said dummy wiring pattern with a replacing insulator, said replacing insulator having a dielectric constant higher than that of an interlayer insulation film isolating a wiring pattern of another layer from said dummy wiring pattern (col3, ll. 28-31, 41-55, and 65-67); and

(c) extracting a value of a parasitic capacitance parasiting said replacing insulator based on a circuit specified by said layout pattern data after replacement with said replacing insulator (col. 2, ll. 30-54; col. 7, ll. 26, ll. 16-42).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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